International Journal of Engineering Sciences Paradigms and Researches (IJESPR)
Volume 47, Issue 01, Quarter 01 (January to March 2018)
An Indexed and Referred Journal with Impact Factor: 2.80
ISSN (Online): 2319-6564
www.ijesonline.com

Modeling, Designing, and Analyzing Photonic Interconnection Networks at both the Physical Layer and System Level

Dr. P. K. Subudhi[1], Rupali Layak[2] and S.Behera[3]

[1]Professor, Department of Computer Science Engineering, Gandhi Institute For Technology (GIFT), Bhubaneswar
[2]Assistant Professor, Department of Computer Science Engineering, Gandhi Engineering College, Bhubaneswar
[3]Assistant Professor, Department of Computer Science Engineering, Gandhi Institute For Technology (GIFT), Bhubaneswar

Publishing Date: 5h March, 2018

Abstract

Photonic technology is becoming an increasingly attractive solution to the problems facing today's electronic chip-scale interconnection networks. Recent progress in silicon photonics research has enabled the demonstration of all the necessary optical building blocks for creating extremely high- bandwidth density and energy-efficient links for on-chip and off-chip communications. From the feasibility and architecture perspective however, photonics represents a dramatic paradigm shift from traditional electronic network designs due to fundamental differences in how electronics and photonics function and behave. As a result of these differences, new modeling and analysis methods must be employed in order to properly realize a functional photonic chip-scale interconnect design. In this paper, we present a methodology for characterizing and modeling fundamental photonic building blocks which can subsequently be combined to form full photonic network architectures. We also describe a set of tools which can be utilized to assess the physical-layer and system-level performance properties of a photonic network. The models and tools are integrated in a novel open-source design and simulation environment. We present a case study of two different photonic networks-on-chip to demonstrate how our improved understanding and modeling of the physical-layer details of photonic communications can be used to better understand the system-level performance impact.

Keywords: *Optical communications, optical crosstalk, optical losses, photonic interconnection networks, simulation software, system analysis and design.*

Introduction

The computing industry has been steadily increasing the number of cores on a single processor performance through parallel computation in order for chip multiprocessor (CMP) systems to properly function and take advantage of the multiple cores, interconnection networks are required to provide both on-chip (e.g., core to core) and off-chip (e.g., core to main memory) communication links. Electronic interconnection networks have thus far been capable of coping with the communication demands of today's applications, however further scaling of the number of cores and memory requirements of applications may not be able to be matched with equivalent communication improvements [1]. This inability of electronic interconnects to scale in performance is a consequence of the large amount of power that is dissipated by the electronic interconnects and the limited heat-dissipation capabilities of current packaging technology. A previous study has shown that over 50% of the dynamic power dissipated in some high-performance microprocessors comes from the interconnects exclusively [2]. These problems will be further exacerbated as the requirements of CMP systems continue to grow, exemplifying the need for an winter connect technology that can deliver energy-efficient high-bandwidth communications. Photonics

technology has emerged as a promising chip-scale interconnects solution to the various challenges facing CMP scaling. Photonic signaling using wavelength division multiplexing (WDM) can enable orders of magnitude higher bandwidth density than electronics which is becoming increasingly constrained by the wire and pin densities that can be achieved [1]. The power dissipation of photonic signaling can be designed to be practically independent of distance and data rate. This allows for high-speed data to flow seamlessly between the on-chip and off-chip domains. All the necessary optical devices for creating chip-scale photonic interconnection networks have been demonstrated using complementary metal oxidesemiconductor (CMOS) compatible fabrication techniques, as described. This compatibility allows them to be economically produced in existing fabrication lines. Moreover, CMOS compatibility allows these optical devices to be directly integrated with electronic digital circuits, providing a flexible and powerful means to create a high-performance interconnect fabric.

In light of these recognized advantages of optics, many challenges still exist in fathoming and creating a chip-scale photonic network. Chip-scale silicon photonics currently provides no means of in-flight buffering and logical processing. The only way to accomplish these tasks is to use optical-electronic-optical (O-E-O) conversion, and do them in the electronic domain. O-E-O conversion is tolerated in switches for large-scale networks; however the additional power dissipation required would have a detrimental impact on chip-scale systems. Signal regeneration is also not easily accomplished in the CMOS-compatible photonic platform, therefore network architecture designs must carefully consider the optical losses to ensure signal integrity throughout the transmission path. Conventional network simulators are not well suited for photonic networks since they are incapable of capturing all the physical and functional details that differentiate photonic devices from their electronic counterparts.

In this paper, we present a methodology for designing, modeling, and analyzing the performance of photonic interconnection networks. Furthermore, this paper highlights several techniques to synergistically study a photonic architecture's system-level properties through physical-layer analysis. We have also developed the PhoenixSim environment which integrates the modeling and analysis aspects of our methodology and has been made publicly available [3]. PhoenixSim is implemented using OMNeT++, a C++-based event-driven simulation environment [4]. Our methodology and PhoenixSim represent a novel set of tools which system architects can use to see how integrated photonics can potentially impact the performance of a particular computing system.

We review related work in the area of photonic network architectures and other simulators and tools that have been developed to model and design them. We present our methodology and outline the design flow supported by PhoenixSim which guides designers from the modeling of the basic silicon photonics devices, through the composition of the devices into a complex interconnection network, to the analysis of the network performance and scalability. We describe our method for modeling photonic devices and overview a library of fundamental building blocks we have implemented. We present a unique set of analysis tools for optimizing photonic interconnection networks. We then discuss two photonic network-on-chip architectures as case studies in Section VI to demonstrate how our methodology can be used to design and understand photonic interconnection networks.

This paper expands upon work that has been published previously [5]. New contributions include: 1) a complete discussion of our proposed design methodology; 2) the modeling of Mach-Zehnder switches in our Photonic Device Library; 3) the expansion of our noise model to handle intra-message crosstalk and receiver noise; and 4) inclusion of serialization/de-serialization (SerDes) power within our power model. We also conduct our case study on new network topologies and include a more extensive set of results and analysis. Lastly, we include an expanded literature review of photonic interconnection network architectures and photonic interconnect computer-aided design (CAD) tools.

Methodology and Design flow overview

The sequence of design stages we employ for modeling photonic interconnection networks primarily consists of six design steps:
1) Specification of the network building blocks;
2) Specification of the target application;
3) Modeling of the network architecture;
4) System-level performance analysis;
5) Physical-layer characterization;
6) Iterative refinement of parameters and design.
Step 1 involves the specification of the fundamental network building blocks that will be used for creating the interconnection network.

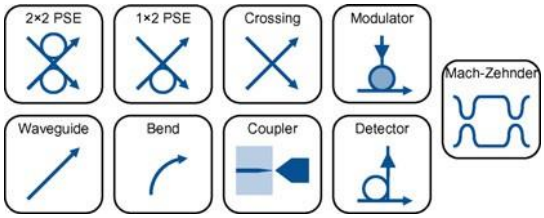

Figure 1: Subset of the photonic devices in the Interconnect Building Block Library

The collection of network building blocks is named the Interconnect Building Block Library. Within this library is a set of photonic devices that are characterized using the Basic Element Device Model (Fig. 1), described in further detail? Users of this design methodology can choose to design a network based on the included library of devices, or extend the library themselves with other novel photonic building blocks.

The library for electronic building blocks consists of switch, arbitrator, and buffer blocks for creating standard pipelined routers. PhoenixSim leverages the Orion simulator for deriving detailed values for electronic delay and energy dissipation. The electronic router model is highly configurable and includes parameters for clock rate, buffer size, channel width, and number of virtual channels. In addition to the standard router design, the electronic router model also includes additional methods for interfacing with photonic devices. Electro-optic photonic devices can take an electronic input to influence its optical behavior and are essential components for enabling the active types of switching used in some proposed networks[6],[12].

Next, Step 2 consists of specifying the target application. PhoenixSim currently supports the use of both synthetically generated traffic patterns and communication traces, with eventual plans for integration with a cycle-accurate microarchitecture simulator. A variety of synthetic patterns have already been created within the environment (e.g., random, hotspot, nearest neighbor, and tornado) and is extensible to others. Communication traces can be generated by monitoring the network traffic during the execution of a real application and used as an input into PhoenixSim. Performance results gained by using communication traces are useful in assessing the application-specific performance gains of photonic networks [15].

The design and modeling of the network occurs in Step 3 of the design flow. The devices from the Interconnect Building Block Library can be combined to create higher-order networking components and entire interconnection network topologies. By accounting for the target applications, a network architect can optimize the topology design to target specific requirements such as message size, latency, and/or throughput. For instance, Fig. 2 illustrates how a nonblocking switch can be derived within PhoenixSim by connecting various devices from the Building Block Library. Step 4 involves the characterization of the network architecture at the physical layer, which involves metrics such as the optical power budget, crosstalk, and power dissipation.

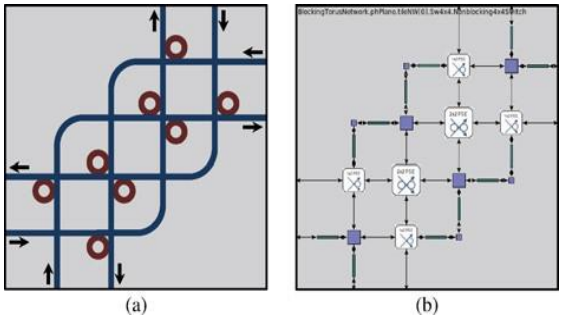

Figure 2 (a) Schematic of a design for a non-blocking photonic switch (b) Screenshot of how PhoenixSim composes the switch by instancing basic photonic devices.

The overall physical-layer performance of a derived photonic component or topology can be determined from the aggregate performance of the individual photonic devices. Although this is not as rigorous as a true link-level simulator, this hierarchical building process enables an accurate first-order physical characterization of an entire network through the characterization of a small number of foundational components.

Step 5 measures the system-level performance characteristics of the network architecture in terms of data throughput and latency. Many of the physical properties that are identified in Step 4 have an impact on network functionality and scalability and play a crucial role in determining overall system performance.
Finally, Step 6 forms the basis for an iterative process, where the performance results and analysis of the modeled network can be used to refine the topology design and device parameters to further optimize the overall performance. Previous work has demonstrated the effectiveness of this iterative step. The initial physical-layer characterizations showed the dramatic impact that waveguide crossing loss had on performance and a subsequent analysis of a system with improved crossings resulted in a dramatic improvement in overall performance [14].

Conclusion

We have described a methodology for modeling, designing, and analyzing photonic interconnection networks at both the physical-layer and system-level. A Photonic Device Library has been devised to describe any type of fundamental photonic elements, which can then be combined and used to model large-scale photonic components and network topologies. We developed a set of physical-layer tools to accurately determine physical properties of the photonic networks and examine how they impact the network architectures in terms of system performance. Our PhoenixSim environment implements this methodology, which we have made open source and publicly available. We illustrated the capabilities of PhoenixSim through the analysis of two photonic networks and showed how various system-level design tradeoffs are made possible through an understanding of the physical layer characteristics. The device library, analysis tools, and simulation environment form a comprehensive design flow for understanding and designing photonically enabled computing systems.

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